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TITLE: SEMICONDUCTOR MEMORY CONTROLLER

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ABSTRACT:

PURPOSE: To provide a semiconductor memory controller, which can control plural semiconductor memory cells, concerning the semiconductor memory controller to compress/expand data.

CONSTITUTION: A semiconductor memory controller 10 is provided with a compression encoder 14 to compress data to be written in semiconductor memories 12 and an expansion decoder 16 to expand data read from the semiconductor memories 12. On the other hand, the semiconductor memory controller 10 is provided with a control circuit 18 to control these compression encoder 14 and expansion decoder 16 and a parameter register group 20 to deisgnate the operating mode of the control circuit 18. Further, this control circuit 18 generates local addresses or various control signals to be supplied to the semiconductor memories 12. Thus, the plural semiconductor memories can be simultaneously managed and efficiently utilized.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the semiconductor memory controller applied to the semiconductor memory equipment which used the semiconductor memory component.
[0002]
[Description of the Prior Art] In recent years, the engine performance of a copying machine, an image display device, etc. is improving remarkably. What has a very big capacity of the semiconductor memory for holding image data etc. in connection with it is demanded. Therefore, the number of the memory devices used for these equipments is huge, and a component-side product is also size very much. Although what is necessary is just to have increased the storage capacity per piece in order to decrease the number of memory devices, as long as there was no fast improvement in the accumulation consistency of a semiconductor memory component, it was inadequate for solving a problem.
[0003] As opposed to such a problem, the memory device with compression / elongation function of data is proposed in JP,63-183699,A, JP,2-86267,A, JP,3-105789,A, etc. By performing compression and elongation of data in each semiconductor memory, many data are memorized with small memory capacity.
[0004]
[Problem(s) to be Solved by the Invention] If the conventional memory device with compression / elongation function was not equipped with the circuit of compression or elongation for every memory device and it was ****, it had the futility that the circuit which carries out ** and the same actuation was [two or more] necessary.
[0005] Moreover, since the code length after compression changes with the data to compress when a variable-length-coding method is adopted as a compression method, the actual storage region used will change with each memory devices. For this reason, the amount of data memorized by each memory device came apart, and there was a problem that efficient use of the storage region of a memory device could not be attained.
[0006] This invention was made in view of such a technical problem, it is the semiconductor memory controller which performs compression and elongation of data, and the purpose is obtaining the semiconductor memory controller which can control two or more semiconductor memory components.
[0007]
[Means for Solving the Problem] A compression means to compress the data inputted into said each memory in order that this invention may solve an above-mentioned technical problem, The control means which generates the address with which it is an elongation means to elongate the data outputted from said each memory, and a means to perform quota control of the storage region in said memory according to said compressed amount of data, and said storage region is expressed, An implication and said two or more memory devices are semiconductor memory controllers

characterized by being prepared in another object.
[0008] Therefore, it is the semiconductor memory controller which realizes close and the memory apparatus to output, and in which the so-called sequential access is possible for close and the data to output for every sequence of the continuously.
[0009] Moreover, a compression means to compress the data by which this invention is inputted into said each memory, They are an elongation means to elongate the data outputted from said each memory, and a means to perform quota control of the storage region in said memory of said compressed data. It is the semiconductor memory controller characterized by preparing said two or more memory devices in another object including the control means which calculates the address with which said storage region is expressed based on the address inputted from the outside.
[0010] Therefore, it is the semiconductor memory controller which specifies the location memorized with the address and which realizes the memory apparatus in which the so-called random access is possible.
[0011]
[Function] Conventionally, compression / elongation means was established for every semiconductor memory component. However, since only the lot is prepared in the semiconductor memory controller of the piece which manages two or more semiconductor memory, compression / elongation means in this invention can perform the data compression and elongation to all semiconductor memory components with compression / elongation means of the lot. Moreover, since two or more semiconductor memory is managed by the semiconductor memory controller of a piece, it is 1 base-tube Michiyoshi ability about the operating condition of two or more semiconductor memory components.
[0012]
[Example]
One or less example and the suitable example of this invention are explained based on a drawing.
[0013] The configuration block Fig. of the memory apparatus which applied the semiconductor memory controller which is one example of this invention to drawing 1 is shown. This memory apparatus consists of a semiconductor memory controller 10 which is one example of this invention, and semiconductor memory 12 which memorizes the data compressed by the semiconductor memory controller 10, and I/O of data is altogether performed through this semiconductor memory controller 10 as shown in drawing.
[0014] The semiconductor memory controller 10 is equipped with the compression encoder 14 which compresses the data which should be written in semiconductor memory 12, and the elongation decoder 16 which elongates the data read from semiconductor memory 12. Moreover, the semiconductor memory controller 10 is equipped with the control circuit 18 which controls these compression encoders 14 and elongation decoders 16, and the parameter register group 20 which specifies the mode of operation of a control circuit 18. This control circuit 18 generates the partial address further supplied to semiconductor memory 12, and various control signals. These addresses and signals are supplied to each semiconductor memory 12 by the partial address bus 22, local-control bus 24, etc.
[0015] The memory apparatus using the semiconductor memory controller 10 shown in drawing 1 does close and the output of data by the command from CPU which is not illustrated. This memory apparatus can be operated by various modes of operation by the parameter register group 20 mentioned above. When they divide roughly, they are a sequential entry of data, an output, and a random entry of data and an output. Hereafter, the actuation is explained to a detail about those modes.
[0016] (a) It is inputted in fixed sequence from a sequential entry of data, an output CPU, etc., and there is a thing like image data in the data which are outputted only in the same sequence as it and with which the so-called sequential access is made. In

image data etc., data are outputted and inputted for every party like [in the case of displaying, for example on the CRT display of a raster scan mold]. That is, this example is an example in the case of being used for a frame memory, an image data buffer, etc. of a CRT display.

[0017] In a sequential entry of data, each sequential data inputs into the semiconductor memory controller 10 one by one from CPU etc. Since only the sequence is important in sequential data, the address is not supplied from CPU etc. The inputted data are written in semiconductor memory 12 through the partial data bus 26, after predetermined compression is performed by the compression encoder 14. The partial address at the time of being written in is generated by the control circuit 18, and is supplied to semiconductor memory 12 through the partial address bus 22. The increment of this partial address is carried out according to the compressed data length after compression of each data. This partial address by which the increment was carried out is held at the write-in pointer in the write-in pointer control circuit 18, and is used in the case of the following entry of data.

[0018] Thus, in a sequential entry of data, since the address is not specified, a control circuit 18 can determine the partial address independently of the exterior. Therefore, it is possible to use the variable-length-coding method with which not only the fixed-length-coding method whose compressed data length after compression is immobilization but compressed data length does not become fixed die length. Generally, the way of a variable-length-coding method has high compressibility, and this coding method is used abundantly at compression of image data.

[0019] The control circuit 18 has the pointer which it not only generates the partial address at the time of writing in semiconductor memory 12, but holds the partial address which began writing. This pointer is read and a pointer is called. The partial address which this read-out pointer holds in the case of the output of sequential data is supplied to semiconductor memory 12. The expanding decoder 16 develops, the original data are restored, and the read compressed data is outputted outside.

[0020] As stated above, if an external circuit inputs only in sequence and reads [as opposed to / only / the semiconductor memory controller 10] after that, in I/O of sequential data, the output of data will be performed in the same sequence. In this example, although it is possible to use a variable-length-coding method as mentioned above, from the outside, it cannot judge what magnitude in the case of this coding method, the amount of actual compressed data becomes. Therefore, if any allowance is not made, either, there is a possibility of it becoming impossible to perform an entry of data when the amount of data storages exceeds the total memory capacity of semiconductor memory 12, and destroying the data which input before and are not read yet. The control circuit 18 in this example is always supervising the rate of the actual data memorized to the total memory capacity, and if the rate becomes beyond a fixed value, it will output an alarm signal outside. This alarm signal can be used for the interruput signal over external CPU etc. In addition, the value of the rate used as the criteria of this decision can be specified through the parameter register group 20 from the exterior. In addition, this monitor can be easily attained by comparing the partial address currently held at the read-out pointer with the partial address by which write-in pointer maintenance is carried out.

[0021] (b) Many [to the data which specify the address, i.e., the location written in, and are inputted from a random entry of data, an output CPU, etc. and with which the so-called random access is made / usual alphabetic data, a usual array, etc.] Moreover, a thing like the image data described in explanation of sequential data also has the case where he wants to take out some images alternatively etc., and, in such a case, it is common to be convenient in access which specified the address being possible. In such random access, since the location written in is specified in the address, a variable-length-coding method is inapplicable. However, since the partial address with which the compressed data is stored is determined as a meaning from the

address given from CPU etc., a fixed-length-coding method can be applied to random access. In this example, the partial address is calculated by the control circuit 18 from the address from the outside. Thus, random data as well as sequential data are compressible by applying a fixed-length-coding method.

[0022] In a random entry of data, each random data inputs into the semiconductor memory controller 10 from CPU etc. with the address. Inputting the address into a control circuit 18, a control circuit 18 calculates the partial address supplied to semiconductor memory 12 based on the address. Moreover, as for data, the data with which fixed length coding was performed and was compressed with fixed compressibility are written in semiconductor memory 12 by the compression encoder 14.

[0023] For example, if the partial address is generated by setting the address from the outside to one half by the coding method which has one half of compressibility, it is possible to memorize twice as many data as the total capacity of the actual semiconductor memory 12. Or it is suitable as for 1/2 in the number of bits of each data, using the address from the outside as the partial address as it is.

[0024] Thus, in a random entry of data, it is easily computable in the partial address supplied to semiconductor memory 12 based on the address from the outside.

[0025] In the output of random data, similarly, the partial address is calculated by the control circuit 18 and semiconductor memory 12 is supplied. The expanding decoder 16 develops, the original data are restored, and the read compressed data is outputted outside.

[0026] Since the address and the partial address from the outside were made to correspond to a meaning in I/O of random data using a fixed-length-coding method as stated above, it is possible to compute the partial address easily from the address from the outside. Therefore, also in random data, I/O of the data based on compression and elongation is possible like the case of sequential data.

[0027] (c) In mixture this example in the mode, although the I/O by compression and elongation of sequential data and random data is possible as mentioned above, it is possible by dividing the storage region by semiconductor memory 12, and considering as the field for sequential data, and the field for random data, respectively to treat two kinds of data to coincidence. Moreover, the usual data which do not carry out compression and elongation depending on the case may be outputted and inputted. It is possible to divide and prepare these fields in the total storage region. a setup in these modes writes a predetermined value in the parameter register group 20 -- or it is attained by setting a flag.

[0028] Since the semiconductor memory component prepared the compression encoder and the elongation decoder conventionally prepared for every semiconductor memory component in another object, it being characteristic in this example is being able to manage two or more semiconductor memory unitary. Therefore, as mentioned above, division of the field to the total memory capacity, the output of the alarm signal accompanying the increment in the amount of data to a storage region, etc. can be realized easily.

[0029] Hereafter, the application of the semiconductor memory controller by this invention is shown by the application 3 from an application 1.

[0030] Application 1 drawing 2 is the configuration block Fig. of the image printer which applied the semiconductor memory controller 30 by this application.

[0031] In an image printer, the image memory 32 which once accumulates image data has large-capacity-ized with the big-screen-izing and high-resolution-izing in recent years. This example uses the semiconductor memory controller 30 by this invention for this image memory 32. The image printer of this example accumulates the image data sent out from a computer etc. in an image memory 32 through the input interface 34. This image memory 32 consists of a semiconductor memory controller 30 by this invention, and semiconductor memory 36 managed by it. The image data accumulated

in this image memory 32 is read one by one, and various image processings are performed by the image-processing circuit 38. Next, it is sent out to the printer device section 42 by the record control circuit 40, and image data is printed on paper etc.
[0032] In this application, the data which the semi-conductor controller 30 treats are mainly sequential data. Each image data sent out from the input interface 34 is compressed, respectively, and is memorized by semiconductor memory 36. In case this image data by which compression storage was carried out is read by the image-processing circuit 38, it is elongated and it is returned to the original image data. In the case of this read-out, it is also possible to perform random access because of edit processings, such as partial logging of an image and rotation of an image.
[0033] Since the direction of an input and an output is fixed, it being characteristic in this application is that the semiconductor memory controller 30 is separately equipped with an input data terminal and an output-data terminal. That is, it is that the input and the output are separately performed independently like the so-called dual port RAM. Before the print of a front image is completed by considering as such a configuration, it is possible to capture the following image from a computer etc.
[0034] Although the terminal with separate input data terminal and output-data terminal is used in this way in this application, when an input and an output are not performed to coincidence, it is also possible to share both the data terminal. Saving of the number of terminals can be aimed at by using in common.
[0035] Moreover, the alarm signal stated in the example 1 is used for control signals, such as busy control to the computer which is a host, in this application. It is possible for a computer etc. to become possible [waiting until an opening comes out to an image memory], and to control a printer by this good.
[0036] Since the semiconductor memory controller 30 which performs compression and elongation of data was used for the image memory 32 of an image printer according to this application as stated above, it is possible to lessen semiconductor memory 36. Therefore, the substrate inside an image printer can be constituted small and effect is taken to reduction of cost.
[0037] Application 2 drawing 3 is the configuration block Fig. of the reproducing unit which applied the semiconductor memory controller 50 by this application.
[0038] In the reproducing unit, various functions by digital processing are added with multi-functionalization by digital processings various in recent years. In such a reproducing unit, the image memory 52 which once accumulates image data has large-capacity-ized like the image printer of an application 1. This application uses the semiconductor memory controller 50 by this invention for this image memory 52. The reproducing unit of this application accumulates the image data read in the manuscript by the reading section 54 in an image memory 52. This image memory 52 consists of a semiconductor memory controller 50 by this invention, and semiconductor memory 56 managed by it. The image data accumulated in this image memory 52 is read one by one, and various image processings are performed by the image-processing circuit 58. The image data after this processing is sent out to the Records Department 60, and image data is copied on paper etc. Although read-out of this image is usually performed in a sequential access, it is also possible to perform random access for edit processings, such as partial logging of an image and rotation of an image.
[0039] In this application, the data which the semi-conductor controller 50 treats like an application 1 are mainly sequential data. Moreover, similarly, in this application, since the direction of an input and an output is fixed, the semiconductor memory controller 50 is separately equipped with the input data terminal and the output-data terminal, and the input and the output are separately performed independently like the so-called dual port RAM. Before the print of a front manuscript is completed by such configuration, it is possible to read the following manuscript. Since the semiconductor memory controller 50 which performs compression and elongation of data was used for the image memory 52 of a reproducing unit according to this application as stated

above, it is possible to lessen semiconductor memory 56. Therefore, the substrate inside a reproducing unit can be constituted small and effect is taken to reduction of cost.

[0040] An application 3 and the semiconductor memory controller by this invention can be used also in case the frame memory used for image display devices, such as CRT, etc. is constituted.

[0041] Various things, such as a liquid crystal type image display device and a plasma display, are developed besides CRT, high-resolution-izing, colorization of a liquid crystal display, etc. take an image display device for progressing, and it has also large-capacity-ized the frame memory in recent years.

[0042] The application 1 mentioned above also in this frame memory and the same configuration as 2 can be adopted, and it is possible to do so same operation and effectiveness. Therefore, the substrate of a frame memory can be constituted small and effect is taken to reduction of cost.

[0043]

[Effect of the Invention] Since the semiconductor memory component formed compression and the means to elongate of data in another object according to this invention as stated above, to two or more semiconductor memory components, it is only compression / elongation means of a lot, and said semiconductor memory group can be managed collectively.

[0044] Therefore, it is possible to manage efficiently the storage region of two or more semiconductor memory components. Therefore, it has the effectiveness that reduction of cost and the miniaturization of equipment can be attained by efficient use of a semi-conductor storage element.

[Translation done.]